AMENDMENTS TO THE SPECIFICATION

Kindly amend paragraphs **[0011]**, **[0023]**, **[0074]**, **[0082]**, **[0084]**, **[0086]**, **[0087]**, **[0090]**, **[0092]**, and **[0105]** of the specification as follows:

[0011] Nodes between the innermost level 0 and the outermost level J communicate message data and control signals among other nodes. For example, a node A on a level T that is neither level 0 or level J receives message data from a node B on level T and also receives message data from a node C on level T+1. Node A sends message data to a node D on level T and also sends message data to a node E on level T-1. Node A receives a control input signal from a node F on level T-1. Node A sends a control signal to a node G on level T+1.

Level M has 2^{J-M} rings, each containing $2^M K$ nodes for a total of $2^J K$ nodes on level M. Specifically:

Level 0 has 2^J rings, each containing $2^0 K = K$ nodes for a total of $2^J K$ nodes on level 0.

Level 1 has 2^{J-1} rings, each containing $2^1 K = 2K$ nodes for a total of $2^J K$ nodes on level 1.

Level 2 has 2^{J-2} rings, each containing $2^2 K = 4K$ nodes for a total of $2^J K$ nodes on level M.

Level J-2 has $2^{J-(J-2)} = 4$ rings, each containing $2^{(J-2)}K$ nodes for a total of $2^J K$ nodes on level J-2.

Level J-1 has $2^{J-(J-1)} = 2$ rings, each containing $2^{(J-1)}K$ nodes for a total of $2^J K$ nodes on level J-1.

Level J has $2^{J-J} = 1$ ring containing $\cancel{2^{(J-1)}K}$ $\underline{2^{(J-0)}K}$ nodes for a total of $2^J K$ nodes on level J.

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[0023] Node A sends control information to a device G. If node A is on the outermost level r=J, then device G is positioned outside of the interconnect structure. Device G is a device, for example a computational unit, that sends message data to node D. If node A is not positioned on level r=J, then device G is a node which is located at node position $\cancel{N(r+1,\theta,h_{r+1}(z))}$ $\underline{N(r+1,\theta,h_r(z))}$ on level r+1 and device G sends message data to node D.

[0074] If node $A(r,\theta,z)$ **530** is on the outermost level r=J, node $A(r,\theta,z)$ **530** is interconnected with a device (e.g. a computational unit) outside of the interconnect structure. Otherwise, node $A(r,\theta,z)$ **530** is interconnected with a node ~~$G(r+1,\theta,h_{r+1}(z))$~~ $\underline{G(r+1,\theta,h_r(z))}$ **542** on level r+1 which receives a control input signal from node $A(r,\theta,z)$ **530**--.

[0082] The devices $CU(\theta,z)$ are also connected to nodes $N(J,\theta,z)$ at the outermost cylinder level. In particular, the data output terminal **406** of devices CU(è,z) are connected to the second data input terminal **212** of nodes $N(J,\theta,z)$. The control bit input terminal **404** of devices $CU(\theta,z)$ are connected to the control output terminal **224** of nodes $N(J,\theta-1,H_J(z))$. Messages are communicated from devices $CU(\theta,z)$ to nodes $N(J,\theta,z)$ at the outermost cylindrical level J. Then messages move sequentially inward from the outermost cylindrical level J to level J-1, level J-2 and so forth ~~unit~~ <u>until</u> the messages reach level 0 and then enter a device. Messages on the outermost cylinder J can reach any of the 2^J rings at level zero. Generally, messages on any cylindrical level T can reach a node on 2^T rings on level zero.

[0084] The nodes $N(T,\theta,z)$ **450** also have a second data input terminal **212** and a second data output terminal **222** which are connected to nodes **102** on the same level T. The second data input terminal **212** of nodes $N(T,\theta,z)$ **450** are connected to the second data output terminal **222** of nodes $N(T,\theta-1,H_T(z))$ **456**. The second data output terminal **222** of nodes $N(T,\theta,z)$ **450** are connected to the second data input terminal **212** of nodes $N(T,\theta+1,h_T(z))$ **458**. The cylinder height designation $H_T(z)$ is determined using an inverse operation of the technique for determining height designation $h_T(z)$. The interconnection of nodes from cylindrical height to height (height z to height $H_T(z)$ and height $h_T(z)$ to height z) on the same level T is precisely defined according to a height transformation technique and depends on the particular level T within which messages are communicated. Specifically in accordance with the height transformation technique, the height position z is put into binary form where $z = z_{J-1}2^{J-1} + z_{J-2}2^{J-2} + \ldots + z_T2^T + z_{T-1}2^{T-1} + \ldots + z_12^1 + z_02^0$. A next height position $h_T(z)$ is determined using a process including three steps. First, binary coefficients starting with coefficient z_0, up to and but not including coefficient z_T are reversed in order while coefficients z_T and above are kept the same. Thus, after the first step the height position becomes $z_{J-1}2^{J-1} + z_{J-2}2^{J-2} + \ldots + z_T2^T + z_02^0 + z_12^1 + \ldots + z_{T-2}2^{T-2} + z_{T-1}2^{T-1}$. Second, an odd number modulus 2^T, for example one, is

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added to the height position after inversion. Third, circularity of the height position is enforced by limiting the inverted and incremented height position by modulus 2^T. Fourth, the first step is repeated, again inverting the binary coefficients below the z^J coefficient of the previously inverted, incremented and limited height position. The inverse operation for deriving height descriptor $H_T(z)$ is determined in the same manner except that, rather than adding the odd number modulus 2^T to the order-inverted bit string, the same odd number modulus 2^T is ~~added to~~ subtracted from the order-inverted bit string.

[0086] When messages are sent from second data output terminal **222** of a node $N(T,\theta,z)$ **450** to a second data input terminal **212** of a node $N(T,\theta+1,h_T(z))$, a control code is also sent from a control output terminal **224** of the node $N(T,\theta,z)$ **450** to a control input terminal **214** of a node ~~$N(T+1,\theta,h_{T+1}(z))$~~ $\underline{N(T+1,\theta,h_T(z))}$, the node on level T+1 that has a data output terminal connected to a data input terminal of node $N(T,\theta+1,h_T(z))$. This control code prohibits node ~~$N(T+1,\theta,h_{T+1}(z))$~~ $\underline{N(T+1,\theta,h_T(z))}$ from sending a message to node ~~$N(T,\theta+1,h_{T+1}(z))$~~ $\underline{N(T,\theta+1,h_T(z))}$ at the time node $N(T,\theta,z)$ **450** is sending a message to node ~~$N(T,\theta+1,h_{T+1}(z))$~~ $\underline{N(T,\theta+1,h_T(z))}$. When node ~~$N(T+1,\theta,h_{T+1}(z))$~~ $\underline{N(T+1,\theta,h_T(z))}$ is blocked from sending a message to node ~~$N(T,\theta+1,h_{T+1}(z))$~~ $\underline{N(T,\theta+1,h_T(z))}$, the message is deflected to a node on level T+1. Thus, messages communicated on the same level have priority over messages communicated from another level.

[0087] The second data output terminal **222** of nodes $N(T,\theta-1,H_T(z))$ are connected to a second data input terminal **212** of nodes $N(T,\theta,z)$ **450** so that nodes $N(T,\theta,z)$ **450** receive messages from nodes $N(T,\theta-1,H_T(z))$ that are blocked from transmission to nodes ~~$N(T-1,\theta,H_T(z))$~~ $\underline{N(T-1,\theta,H_{T-1}(z))}$. Also, the control output terminal **224** of nodes $N(T-1,\theta,H_T(z))$ are connected to the control input terminal **214** of nodes $N(T,\theta,z)$ **450** to warn of a blocked node and to inform nodes $N(T,\theta,z)$ **450** not to send data to node $N(T-1,\theta+1,z)$ at this time since no node receives data from two sources at the same time.

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[0090] Referring to **Figure 14** in conjunction with **Figure 13**, interconnections of nodes **102** on cylindrical level two further exemplify described interconnections. In **Figure 14**, a level two message path **620** is shown overlying the paths **610** and **612** of messages moving on level one. The number of ~~nodes~~ angles K at a cylindrical level is five and the number of ~~levels~~ heights 2^J is 2^2, or 4, for a three level (J+1) interconnect structure **500**. Same-level interconnections of nodes $N(2,\theta,z)$ include: (1) a second data input

terminal **212** connected to the second data output terminal **222** of nodes ~~N(2,θ-1,h_2(z))~~ N(2,θ-1,H_2(z)) and (2) a second data output terminal **222** connected to the second data input terminal **212** of nodes ~~N(2,θ+1,H_2(z))~~ N(2,θ+1,h_2(z)). For nodes N(2,θ,z) on level two, height z differs from height h_2(z) and height H_2(z) only in the final two bit positions. Generally stated in binary form for any suitable number of nodes K at a height and number of heights 2^J in a level, z and z'=h_2(z) on cylindrical level two are related as follows:

$[z_{J-1}, z_{J-2}, \ldots, z_2, 0, 0]' = [z_{J-1}, z_{J-2}, \ldots, z_2, 1, 0]$;

$[z_{J-1}, z_{J-2}, \ldots, z_2, 1, 0]' = [z_{J-1}, z_{J-2}, \ldots, z_2, 0, 1]$;

$[z_{J-1}, z_{J-2}, \ldots, z_2, 0, 1]' = [z_{J-1}, z_{J-2}, \ldots, z_2, 1, 1]$; and

$[z_{J-1}, z_{J-2}, \ldots, z_2, 1, 1]' = [z_{J-1}, z_{J-2}, \ldots, z_2, 0, 0]$.

[0092] Referring to **Figure 15**, interconnections of nodes **102** on cylindrical level three show additional examples of previously described interconnections. A level three message path **720** is shown overlying the paths **710**, **712**, **714**, and **716** of messages moving on level two. The number of nodes K at a cylindrical height is seven and the number of heights 2^J is 2^3 (8), for a four level (J+1) interconnect structure. Same-level interconnections of nodes N(3,θ,z) include: (1) a second data input terminal **212** connected to the second data output terminal **222** of nodes ~~N(3,θ-1,h_3(z))~~ N(3,θ-1,H_3(z)) and (2) a second data output terminal **222** connected to the second data input terminal **212** of nodes ~~N(3,θ+1,H_3(z))~~ N(3,θ+1,h_3(z)). For nodes N(3,θ,z) on level three, height z differs from height h_3(z) and height H_3(z) only in the final three bit positions. Generally stated in binary form for any suitable number of nodes K at a cylindrical height and number of heights 2^J in a level, bits z and z'=h_3(z) on cylindrical level three are related as follows:

$[z_{J-1}, z_{J-2}, \ldots, z_3, 0, 0, 0]' = [z_{J-1}, z_{J-2}, \ldots, z_3, 1, 0, 0]$;

$[z_{J-1}, z_{J-2}, \ldots, z_3, 1, 0, 0]' = [z_{J-1}, z_{J-2}, \ldots, z_3, 0, 1, 0]$;

$[z_{J-1}, z_{J-2}, \ldots, z_3, 0, 1, 0]' = [z_{J-1}, z_{J-2}, \ldots, z_3, 1, 1, 0]$;

$[z_{J-1}, z_{J-2}, \ldots, z_3, 1, 1, 0]' = [z_{J-1}, z_{J-2}, \ldots, z_3, 0, 0, 1]$;

$[z_{J-1}, z_{J-2}, \ldots, z_3, 0, 0, 1]' = [z_{J-1}, z_{J-2}, \ldots, z_3, 1, 0, 1]$;

$[z_{J-1}, z_{J-2}, \ldots, z_3, 1, 0, 1]' = [z_{J-1}, z_{J-2}, \ldots, z_3, 0, 1, 1]$;

$[z_{J-1}, z_{J-2}, \ldots, z_3, 0, 1, 1]' = [z_{J-1}, z_{J-2}, \ldots, z_3, 1, 1, 1]$; and

$[z_{J-1}, z_{J-2}, \ldots, z_3, 1, 1, 1]' = [z_{J-1}, z_{J-2}, \ldots, z_3, 0, 0, 0]$.

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[0105] Nodes N(T,θ,z) include logic that controls routing of messages based on the target address of a message packet M and timing signals from other nodes. A first logic

switch (not shown) of node N(T,θ,z) determines whether the message packet M is to proceed to a node N(T-1,θ+1,z) on the next level T-1 or whether the node N(T-1,θ+1,z) is blocked. The first logic switch of node N(T,θ,z) is set according to whether a single-bit blocking control code sent from node N(T-1,θ,H_{T-1}(z)) arrives at node N(T,θ,z) at a time t_0. For example, in some embodiments the first logic switch takes a logic 1 value when a node N(T-1,θ+1,z) is blocked and a logic 0 value otherwise. A second logic switch (not shown) of node N(T,θ,z) determines whether the message packet M is to proceed to a node N(T-1,θ+1,z) on the next level T-1 or whether the node N(T-1,θ+1,z) is not in a suitable path for accessing the destination device CU(θ_2,z_2) of the header of the message packet M. The header of the message packet M includes the binary representation of destination height z_2 ($z_{2(J)}$, $z_{2(J-1)}$, . . . , $z_{2(T)}$, . . . , $z_{2(1)}$, $z_{2(0)}$. The node N(T,θ,z) on level T includes a single-bit designation z_T of the height designation z (z_J, z_{J-1}, . . . , z_T, . . . , z_1, z_0). In this embodiment, when the first logic switch has a logic 0 value and the bit designation $z_{2(T)}$ of the destination height is equal to the height designation z_T, then the message packet M proceeds to the next level at node N(T-1,θ+1,z) and the destination height bit $z_{2(T)}$ is stripped from the header of message packet M. Otherwise, the message packet M traverses on the same level T to node N(T,θ+1,h_T(z)). If message packet M proceeds to node N(T-1,θ+1,z), then message packet M arrives at a time $t_0 + (\alpha - \beta)$ which is equal to a time $(z_2 - z_1 + 1)\alpha + (J - 1)\beta$. If message packet M traverses to node N(T,θ+1,h_T(z)), then message packet M arrives at a time $t_0 + \alpha$, which is equal to a time $(z_2 - z_1 + 1)\alpha + J\beta$. As message packet M is sent from node N(r,θ,z) to node N(T,θ+1,h_T(z)), a single-bit control code is sent to node ~~N(T+1,θ+1,H_{T+1}(z))~~ N(T+1,θ,h_T(z)) (or device CU(θ,z) which arrives at time $t_0 + \beta$. This timing scheme is continued throughout the interconnect structure, maintaining synchrony as message packets are advanced and deflected.

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